Parth Rajeshkumar Thakkar

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EDUCATION

University of Colorado Boulder, Boulder, CO — Aug, 2023 - May, 2025
Master's of Science, Embedded Systems Engineering & IoT — GPA: 3.80 / 4.0

Courses: Principles of Embedded Systems, Embedded System Design, Internet of Things & Embedded Firmware (IoTF), PCB Design, Real-Time Embedded Systems, Low-power Embedded systems, Concurrent Programming

L.D. College of Engineering, Ahmedabad, India — Jun, 2019 - May, 2023
Bachelor's of Engineering, Electronics and Communication — GPA: 8.67 / 10.0

WORK EXPERIENCE

Advanced Micro Devices (AMD) — May, 2024 - Aug, 2024
Firmware Developer, Intern — Austin, TX

- Contributed to firmware development for next-generation APUs and CPUs (Strix, Strix Halo, GraniteRidge), resolving 300+ UEFI core bugs and a critical corrupted code recovery issue, significantly enhancing system stability and reliability.
- Helped in boot time optimization, achieving 15% improvement through implementation of advanced compression algorithms and SPI DMA.
- Orchestrated TianoCore patching for AMD-specific requirements and reduced coverity static error to 60% across all the modules critical GCC/Makefile errors, enabling seamless single module builds for cross-platform monorepos.
- Contributed to code reviews and CI/CD processes, enhancing development efficiency
- Developed QEMU UEFI Drivers to gain in-depth understanding of UEFI development technicalities, bolstering firmware development capabilities and contributing to the team's knowledge base.

Griden Power — Sep, 2022 - Aug, 2023
Embedded Developer, Intern — Ahmedabad, India

- Implemented MQTT (Message Queue Telemetry Transport) and OCPP 2.0 (Open Charge Point Protocol) for a Level 2 DC fast charger, enabling seamless data transmission and reducing downtime by 40%.
- Developed a high-speed PCB with a ground plane and return vias on switching, which **reduced up to 20%** of ground bounce and switching noise, thereby enhancing signal integrity.
- Integrated FreeRTOS with ESP32 to leverage its dual-core architecture for doubled the efficiency.

Robocon LDCE — Jun, 2019 - May, 2023
Hardware Developer — Ahmedabad, India

- Wrote drivers for ATMega328p, integrating various communication protocols like I2C, UART, and SPI. Led PID control and motor drivers to create an efficient control system for a complex robot that represented the university in the National-level DD Robocon competition (Robo Rugby).
- Led the team to successfully secure the 5th position in the competition.

SKILLS

- **Programming Languages:** C, C++, Assembly, Python, Verilog, Shell Scripting
- **Hardware:** Altium (Schematic Capture & Layout), Datasheets, Reference Manuals, Soldering, Hardware Prototyping
- **Microcontrollers:** 8051, MSP430, KL25Z, 8086, STM32F0/F4, ATMega328p, Blue Gecko (EFR32BG13), ESP32c3
- **Architectures:** ARM Cortex-M0/M4, AVR, x86, RISC
- **Communication Protocols:** UART, I2C, SPI, RS232, PS2, RF (BLE, WiFi), USB, Ethernet, CAN
- **Development Tools:** GDB, Valgrind (Memory Debugging), Logic Analyzer, Oscilloscope, Make, CMake, Git, POSIX
- **Operating Systems:** FreeRTOS, Linux (Debian), Windows, Embedded Linux
- **Skills:** OOP, Multithreading, Concurrent Programming, System Programming, JTAG debugging

PROJECTS

Pong game in 8051 using assembly | Link

- Using assembly code, coded a Pong game for the 8051 microcontroller, integrated a custom-designed **PS/2 keyboard hardware** controller for paddle control and a daisy-chained SPI LED matrix serving as the display.
- Constructed a circuit with a bootloader circuit utilizing AT89C51RC2, created device drivers for 32KB external NVSRAM, bit banged IO expander with I2C using AS31 assembler.

8-bit CPU | Link

- Engineered a CPU composed of basic transistor-transistor logic and logic gates on a breadboard. It is capable of executing basic programs such as Fibonacci series, addition, and subtraction.
- As an embedded system, it is equipped with all necessary core blocks such as program counter, ALU, control unit, LCD for output register, two GPRs, instruction register, soft control unit made in EEPROM (28C256), clock unit, instruction decoder, and a 16-byte RAM address decoder made in purely logic gates.

Bare Metal RTOS in STM32F070 | Link

- Systematized a bare-metal RTOS for an ARM Cortex-M0+ core. Included a number of features, such as a Scheduler, RTOS with Round Robin, Cooperative, and Periodic Scheduler methods. Semaphores and Mutexes were also Designed.